after the substrate is thinned, i.e. after PROCEDURE III or since PROCEDURE IV, only low-temperature processes occur.

7. The method as defined in claim 6, wherein said low temperature is considered to be less than 600 °C.

REMARKS

This is in response to the Office Action mailed on September 25, 2002 in which claims 1-7 were pending. In response to the previous Office Action, Applicant traversed the restriction requirement. Applicant elected the embodiment of claims 6 and 7 and amended claims 2-5 to depend from independent claim 6. In this Office Action, the restriction requirement was made final, and claims 2-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Otsuki et al., U.S. Pat. No. 5,378,903 ("Otsuki") in view of Bartko et al., U.S. Pat. No. 4,278,476 ("Bartko") and Sopori, U.S. Pat. No. 5,304,509. As will become clear from the arguments below, the instant invention is allowable over the cited art. Reconsideration and notice to that effect is respectfully requested.

To understand the differences between the instant invention and the cited art, it would be useful to first consider the instant invention in the context of the prior art. Before the present application's priority date, i.e. before 2000, there were generally only two ways to produce IGBTs. One was the conventional PT-IGBT (punch-through type IGBT) (*See* IEDM Tech. Dig., pp. 264-267, 1982, and IEEE Trans. on Power Electronics, vol. PE-2, no. 3, (1987) pp. 194-207), which contains a very thick backside p+ emitter, an n+ buffer layer, an n+ layer and a frontside structure formed on the topside of the n+ layer. The process sequence of making the IGBT was as follows: starting with a p+ substrate, the n+ buffer layer and n+ layer are formed by epitaxial growth, and the frontside structure was fabricated on the topside of the n+ layer.

The second way to produce IGBTs was the NPT-IGBT technology firstly introduced by Siemens Co. (*See* IEEE PESC Record 1, pp. 21-25, 1989, and Proc. of ISPSD''96, pp. 331-334 and 169-172), where the starting substrate was an n+ wafer instead of p+, and its frontside-structure

was fabricated from the very beginning, followed by the thinning of the n+ layer from the backside, and then the shallow p+ backside emitter was achieved by ion implantation.

There are several notable differences between the conventional PT- and the NPT-IGBTs. First, the fabricating sequence is very different as mentioned above. Second, in the PT-IGBT, there is an n+ buffer layer whereas in the NPT-IGBT there is no buffer layer. Thus, the n+ layer of the NPT-IGBT must be thicker than that of the PT-IGBT to sustain the same high-voltage. With a buffer layer, the thickness of the n+ layer can be reduced, and thereby the on-state voltage and excess carriers stored in the n+ layer can be reduced (an advantage achieved by PT-IGBTs).

Third, generally speaking, the substrate must perform a mechanical sustaining function. Therefore, the p+ layer of the PT-IGBT is the thickest part in its structure. To reduce the series resistance, the p+ substrate of the PT-IGBT must be doped heavily. Compared with the thin and low-doped backside p+ emitter of the NPT-IGBT, the injection efficiencies of the more heavily doped p+ substrate of the PT-IGBT is high, relative to the NPT-IGBT. A lower injection efficiency means a larger electron current through the backside emitter junction, which can help the cleanup of excess carriers in the n+ layer during the turn-off of the IGBT (an advantage was achieved by the NPT-IGBT technology). To further illustrate this point, the ion-implantation-formed, thin and low-doped backside emitter of the NPT-IGBT is also referred to as ""transparent emitter (for electrons)"" or ""weak emitter"" (referring to US Patent 6,242,288 B1).

Fourth, since the injection efficiency of the PT-IGBT is high, an additional irradiation step must be combined to the fabricating sequence to reduce the lifetime of the carriers, which can help the cleanup of excess carriers in n+ layer during turn-off and compensate the loss caused by the high injection efficiency.

Fifth, not using irradiation makes the temperature coefficient of the on-voltage of the NPT-IGBT positive, which is beneficial for parallel connection. By contrast, the temperature coefficient of the on-voltage of the PT-IGBT is negative due to its reduced carrier lifetime (*See* IEEE PESC 1989 Record 1, 1989, pp. 21 -25; Proc. ISPSD''97, 1997, pp. 237-240; and IEEE Trans. Ind. App., vol. 38, no. 1, pp. 168-174)

Sixth, the fabrication cost of the conventional PT is higher than that of the NPT especially for high-voltage IGBTs because the thick-layer epitaxial growth is expensive.

From the above discussion, it can be seen that both the conventional PT and the NPT technology possess their own drawbacks as well as their advantages.

The present invention, however, proposes a third way to produce a new kind of PT-IGBT. Please note that it is a NEW KIND of PT-IGBT, not the conventional PT-IGBT. This new kind of PT-IGBT combines the transparent backside emitter of the NPT and the buffer layer structure of the PT, which also combines the advantages achieved by them, i.e. a high electron current (being beneficial during turn-off), and a low on-voltage, less storage of excess carriers, respectively.

In the fabricating steps of this new kind of PT-IGBTs, the stating substrate is also an n+ wafer just like that in NPT-IGBT technology and not like that in the conventional PT-IGBT. Firstly, a diffused, to be more accurate, a deeply-diffused (from near 100 to 200 microns or so) n+ layer is formed on the backside of the n+ substrate, the residual layer of which will act as a buffer layer in the future structure. Then, the frontside-structure is formed on the topside of the n+ substrate. And then the wafer subjects to a thinning from its backside to result in a residual layer of the previously diffused n+ layer to present a relatively thick and low-doped n-type buffer layer. Finally, the p-type backside emitter is formed by ion implantation thus finishing the main phase of fabrication of the new PT-IGBT.

We use the residual of a diffused layer as the buffer layer for three reasons. (1) This method of introducing the buffer layer avoids the high-cost epitaxial growth of n+ buffer and n+ layer for PT-IGBTs, and makes the whole process compatible to the low-cost fabricating process of the NPT. (2) A residual of a diffused layer can be controlled to be relatively thick (several microns to several tens of microns), and relatively low-doped, which can avoid remarkably affecting the injection efficiency of the backside emitter and overcome the drawbacks of FS IGBTs, whose idea is almost the same as the present invention but its method is not (*See* the specification of the present invention, pp. 2-3). (3) Not using a residual means a shallow diffusion (several microns to several tens of microns) must be carried out. Further, not using a residual means that we must use a thinner

n+ substrate, which tends to break during high-temperature processes because the difference of the substrate thicknesses for deep diffusion and shallow diffusion is of 100 microns or more.

From the above description, it is clear that the present invention is not obvious. The instant invention overcomes many problems to introduce a new generation of IGBT of low loss (both statically and dynamically). At the same time, this idea and its method can be easily applied to the domains of GTOs and MCTs, etc. To our knowledge, the method of the instant invention has not been duplicated or published in the prior art.

In the Office Action, the Examiner rejected claims 2-7 under 35 U.S.C. §103(a) as being unpatentable over Otsuki, in view of Bartko and Sopori. The Otsuki reference is different from the instant invention. Otsuki discloses:

> The semiconductor device is formed of a collector (anode) layer 2 as a p+ type semiconductor substrate with which a collector electrode 1 (anode electrode of a thyristor) conductively contacts as a rear electrode; an n+ type buffer layer 3 formed on the collector layer 2; an n- type base layer 4, as a conductivity modulating layer (drift layer) formed on the buffer layer 3; a p type base region 5 formed in the form of a well in the main face side of the n- type base layer 4; .....

(See Col. 5, Line 61 to Col. 6, Line 1 and FIG. 1). With the starting substrate being p+ and the following fabricating sequence most likely being the epitaxial growth, the Otsuki method appears to be the conventional PT-like method, and does not teach, suggest or disclose the method of claim 6.

With respect to Bartko and Sopori, the conventional process techniques employed in the present invention, such as ion implanting, high-temperature diffusion, annealing/sintering, thinning and polishing, are not new to public. However, what is claimed in Claim 6 of the present invention is NOT the SEPARATE or INDIVIDUAL process steps or techniques mutually independent one by one, but their combination to form a special structure (a new generation of IGBTs). Claim 6 must be evaluated in its entirety, and not independently on a step-by-step basis. None of the cited references teach the whole combination, the whole arrangement, or the whole sequence of the steps of the method, and none of the cited references achieve this new generation of IGBTs. The resultant structure is very creative and very different from the prior art (particularly with respect to the references cited in the specification of the present invention and this reply).

Therefore, independent claim 6 is allowable over the cited art. Reconsideration and notice to that effect is respectfully requested.

Finally, the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type residual diffused-layer recited in pending claims 2-5 and 7 are critical because they determine the injection efficiency of the backside emitter, which is very important for the low switching loss of the new PT-IGBT. And, to a large extent, the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type residual diffused-layer also determine the thickness of n+ layer for sustaining high-voltage, which is also very important for the low on-voltage and for switching loss. In fact, with this newly introduced buffer layer, controlling these parameters presents a NEW CHALLENGE for the semiconductor industry.

Although the claimed ranges of the thickness of the backside p+ emitter, the n-type residual diffused-layer, the implanting dose of the backside p+ emitter, and the doping concentration of the n-type residual diffused-layer may be optimal, they were first discovered and discussed in the instant invention. In summary, the instant invention teaches a method for manufacturing a new generation of IGBTs based on the idea of combining the PT structure and the transparent emitter. This combination is not obvious, but rather requires a deep understanding and perception of the prior art of IGBTs, a creative and careful design of the structure as departing from prior IGBT structures, and elaborate fabricating skills and capabilities. To further supplement the Examiner's understanding of the subject matter of the invention, Applicant submits for the Examiner's reference a scientific journal article (submitted for academic publication, but not yet published) that provides a further detailed description of one of the embodiments of the present invention. The many design and fabrication considerations of the embodiment presented are further evidence of the invention's non-obviousness.

Claims 2-5 and 7 depend from independent claim 6. As previously discussed, independent claim 6 is allowable over the cited art. For this reason, and for the independent

distinctions described above, claims 2-5 and 7 are also allowable over the cited art. Reconsideration and notice to that effect is respectfully requested.

Respectfully submitted,
KINNEY & LANGE, P.A.

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By _____

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